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10/591,192	08/30/2006	Steven T. Peake	GB04 0053 US1	5901

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EXAMINER	
BUDD, PAUL A	
ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,192	PEAKE, STEVEN T.	
	Examiner	Art Unit	
	PAUL A. BUDD	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8 and 10* is/are rejected.

7)☒ Claim(s) *2-4,7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Claims **1-10** are pending in the instant application. The preliminary amendments are entered.

Claim Objections

2. Claim **1** is objected to because of the following informalities: Please change "base contact" to be "body contact" on line 14. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims **1** and **5** are rejected under 35 U.S.C. 102 (b) as being anticipated by Uesugi et al. (US Patent 5,708,286).

Regarding claim **1**, Uesugi discloses a trench field effect transistor (trench-FET) comprising:

a semiconductor body [FIG. 1, 40; column 5 line 35, "semiconductor substrate"] having opposed first [top] and second [bottom] major surfaces;

a source metallization [FIG. 1, 80] at the first major surface [top];

source contact regions [FIG. 1, 50] of semiconductor [as above] doped to have a first

conductivity type [n+] at the first major surface [top] in contact [per FIG. 1] with the source metallization [80];

body contact regions [FIG. 23, p implanted area on the far right side of FIG. 23; implanted at FIG. 21 by column 10 lines 32-37] of semiconductor doped [column 10 lines 32-37] to have a second conductivity type [p] opposite [p versus n] to the first conductivity type [n] at the first major surface [top] in contact [FIG. 23, far right side] with the source metallization [80];

a drain region [FIG.1, 20, 10] of first conductivity type [n] under [bottom] the first major surface [top];

a drain contact [FIG. 1, "D"; column 5 lines 44-46] connected to the drain region [10, 20]; and

insulated gates [FIG. 1, 30, GIS2] including a conductive gate [30] in an insulated trench [FIG. 1, 30, GIS2; FIG. 19-23, 30, GIS2] for controlling current flow [inherently a FET gate] between the source contact region [50] and the drain region [20, 10] through mesa regions [FIG.s 29-30 shows plan view including mesas between trenches] between the insulated gates [FIG. 30; 30],

wherein the source contact regions [50] and base contact regions [same as the body contact region] alternate laterally [per FIG 26-33] across the first major surface [top], with the source contact region [50] arranged in [the source is bounded by the trench and not in direct or electrical contact with the gate electrode as enabled by the applicant] the insulated trench [insulated by GIS2] above the insulated gate [30].

Regarding claim **5**, Uesugi discloses the trench-FET according to claim **1**, wherein the drain regions [20, 10] include a drift region [20] of lower doping [n-] above [spatially above per FIG. 1] a highly doped drain region [10] of higher doping [n+] than the drift region [20, n-], both drain [10] and drift regions [20] being of the first conductivity type [n].

5. Claims **6, 8** and **10** are rejected under 35 U.S.C. 102 (b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as *obvious* over Uesugi et al. (US Patent 5,708,286).

Regarding claim **6**, Uesugi discloses the trench-FET according to claim **5** wherein the doping in the drift region [20] is below $1x10^{17}$ cm^3 [FIG. 1, n-] and the doping in the highly doped drain region [10]is above $1x10^{18}$ cm^3 [n+]. *It is well known in the art to make an n+ region as high as* $1x10^{22}$ *for the purpose of providing good ohmic contact and a n- drift region doping of* $1x10^{15-16}cm^3$ *is also typical concentrations for the breakdown voltages* of Uesugi.

Regarding claim **8**, Uesugi discloses a method of manufacturing a trench-FET, including the steps of:

providing a semiconductor body [FIG. 1, 40; column 5 line 35, "semiconductor substrate"] having opposed first [top] and second [bottom] major surfaces doped [column 9 lines 55-57] to be of first conductivity type [n] to form a drain region [10];

implanting [column 9 lines 55-57] a body contact region [FIG.s 21-23] at the first major

surface [top] of semiconductor doped to be of a second conductivity type [p] opposite to the first conductivity type [n];

forming [column 9 line 44 to column 10 line 31] trenches laterally [FIG.s 26-33] across the first major surface [top] alternating laterally with the body contact regions [as above], the trenches extending below [per FIG.21-23] the body contact regions [as above] defining mesa regions [FIG.s 29-30 shows plan view of mesas] below the body contact regions [FIG. 21-23] between the trenches [GIS2 & 30];

forming insulated gates [30] in the trenches [GIS2 & 30];

depositing [column 9 lines 55-67] source regions [50] of semiconductor doped to be of the first conductivity type [n+] in the trenches [the source is bounded by the trench and not in direct contact with the gate electrode as enabled by the applicant] above [per FIG. 1] the insulated gates [GIS2, 30]; and

depositing [*using deposition techniques to form metallization layer is standard and well known in the industry*] a source metallization [80] at the first major surface [top] contacting the source regions [50] and the body contact regions [FIG. 21-23].

Regarding claim **10**, Uesugi discloses a method according to claim **8** wherein the step of forming insulating gates [GIS2] in the trenches [as above] includes the steps of forming [column 10 lines 21-23 “oxidation”] insulator [GIS2] on the sidewalls and base [as shown] of the trenches, forming [column 10 lines 25-26] gate conductor [30] in the trenches to a depth below [per FIG.s] the top of the trenches and forming [column 10 lines 21-23] gate-source insulator [GIS2] in the trenches above the gate conductor [30].

6. Claims **1, 5** and **6** are rejected under 35 U.S.C. 102 (e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as *obvious* over Schaffer (US Patent 7,253,475).

Regarding claim **1**, Schaffer discloses a trench field effect transistor (trench-FET) comprising:

a semiconductor body [FIG. 3] having opposed first [top] and second [bottom] major surfaces;

a source metallization [FIG. 3, 83] at the first major surface [top];

source contact regions [FIG. 3, 31] of semiconductor doped to have a first conductivity type [n+] at the first major surface [top] in contact [per FIG. 3] with the source metallization [83];

body contact regions [FIG. 3, 34] of semiconductor doped [p+] to have a second conductivity type [p] opposite [p versus n] to the first conductivity type [n] at the first major surface [top] in contact [FIG. 3] with the source metallization [83];

a drain region [FIG. 3, 33] of first conductivity type [n] under [bottom] the first major surface [top];

a drain contact [column 1 line 49 “drain terminal”] connected to the drain region [33]; and

insulated gates [FIG. 3, 41] including a conductive gate [72, 42] in an insulated trench [FIG. 3, 4] for controlling current flow [inherently a FET gate] between the source contact region [31] and the drain region [33] through mesa regions [between adjacent

power devices] between the insulated gates [FIG. 3; 41],

wherein the source contact regions [31] and base contact regions [same as the body contact region] alternate laterally [column 1 lines 12-37 describes multiple power FETs connected in parallel] across the first major surface [top], with the source contact region [31] arranged in [per FIG 3] the insulated trench [4] above the insulated gate [41].

Regarding claim **5**, Schaffer discloses the trench-FET according to claim **1**, wherein the drain regions [lower n+ region not shown] include a drift region [33] of lower doping [n] above a highly doped drain region of higher doping [n+] than the drift region [33], both drain [not shown] and drift regions [33] being of the first conductivity type [n]. It would have been *obvious* to one of ordinary skill in the art at the time that the invention was made to place an n+ region on the backside of the FET of Schaffer for the purpose of providing an n-type region of high enough doping to form an ohmic contact.

Regarding claim **6**, Schaffer discloses the trench-FET according to claim **5** wherein the doping in the drift region [33] is below $1x10^{17}$ cm^3 [FIG. 3, "n"] and the doping in the highly doped drain region [as above] is above $1x10^{18}$ cm^3 [as above]. *It is well known in the art to make an n+ region as high as* $1x10^{22}$ *for the purpose of providing good ohmic contact and a n- drift region doping of* $1x10^{15\text{-}16}cm^3$ *is also typical concentrations for the breakdown voltages* of Schaffer.

Allowable Subject Matter

7. Claims **2-4, 7** and **9** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Paul Budd/

/Jerome Jackson Jr./

Primary Examiner, Art Unit 2815